Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **ADJUST**
2. **N. ON/OFF**
3. **INPUT (2pads)**
4. **GROUND**
5. **OUTPUT (2pads)**

**.129”**

**.080”**

**1 2 4 5**

**5**

**3**

**3**

**MASK**

**REF**

**LM2991D**

**NOTE: Chip back must be connected to Input Voltage.**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Vin**

**Mask Ref: LM2991D**

**APPROVED BY: DK DIE SIZE .080” X .129” DATE: 7/7/22**

**MFG: NATIONAL SEMI THICKNESS .010” P/N: LM2991**

**DG 10.1.2**

#### Rev B, 7/19/02